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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/654,875	09/05/2000	Isao Nojiri	50006-073	7618

7590 05/16/2003

McDermott Will & Emery  
600 13th Street N W  
Washington, DC 20005-3096

EXAMINER
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PAREKH, NITIN

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 05/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/654,875

Applicant(s)

NOJIRI ET AL.

Examiner

Nitin Parekh

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 24 March 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 7-10 is/are pending in the application.
- 4a) Of the above claim(s) 7-9 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 10 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 September 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some \* c) ☐ None of:  
1. ☒ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s) \_\_\_\_\_.  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)  
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other:

## **DETAILED ACTION**

### ***Request for Continued Examination***

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 03/24/03 has been entered. An action on the RCE follows.
2. The amendment filed on 02/25/03 has been entered.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art (APA) in view of Wark et al. (US Pat. 5847445) and Fukui et al. (US Pat. 6100594).

Regarding claim 10, APA teaches a conventional semiconductor device (Fig. 11 and 12; specification pages 2-4) comprising:

- a circuit board (102 in Fig. 11/12)
- a first semiconductor chip (110 in Fig. 11/12) positioned on the circuit board, the first chip being configured to be smaller than the circuit board so that it is confined within an outer periphery of the circuit board
- a second semiconductor chip (112 in Fig. 11/12) positioned on the first semiconductor chip, the second chip being configured to be smaller than the first chip so that it is confined within an outer periphery of the first chip
- the circuit board has a pad/second pad (104-1 in Fig. 12)
- the second semiconductor chip (112 in Fig. 12) has a pad/third pad (114-1 in Fig. 12), positioned closer/adjacent to the second pad, and
- the second pad on the circuit board and the third pad on the second chip are electrically connected through a bonding wire (116 in Fig. 11/12).

The APA fails to teach:

- a) the circuit board having a first pad such that the second pad is spaced away from the first pad in a direction along the outer periphery of the chip, and
- b) the circuit board further having a wire connecting the first and second pads, the wire being printed on the circuit board together with the first and second pads.

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a) Wark et al. teach using a substrate (58 IN Fig. 5; Col. 6, line 64; Col. 10, line 62) such as a printed circuit board (PCB) having a bonding pad/wiring configuration comprising:

- a pad/second bonding pad site (not numerically referenced in Fig. 5- see a bonding pad/site where the bonding wire is connected to a conductive trace/strip 64 located at upper right side on PCB 58 in Fig. 5, shown as a reference numeral 34 in Fig. 1) being electrically connected to a chip with a bonding wire (50 and 62 respectively in Fig. 5), and
- the conductive traces/strips (64 in Fig. 5; Col. 6, line 67) on the PCB being patterned and extended in lengthwise or widthwise direction along an outer periphery of the chip (see 64 being extended in both directions in Fig. 5) such that a bonding site/first pad on the PCB can be located at any point spaced-away/extended from the second bonding pad site/pad in a lengthwise or widthwise direction along outer periphery of the chip (Col. 6, 65- Col. 7, line 20).

b) Fukui et al. teach forming a wiring portion/trace pattern on a circuit board/substrate using a metal deposition and photolithography/printing processes (Col. 7, line 30-60).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a circuit board having a first and second pads such that the second pad is spaced away from the first pad in a direction along outer periphery of the chip as taught by Wark et al. and a wire being printed on the board connecting the first and second pad as taught by Fukui et al. so that the bonding wire length and wire bonding defects can be reduced and the electrical connection towards the outer periphery of the substrate can be accomplished APA.

#### ***Response to Arguments***

5. Applicant's arguments with respect to claim 10 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers

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for the organization where this application or proceeding is assigned are 703-308-7722, 703-308-7724 or 703-872-9318 (Right FAX) for regular communications; 703-872-9310 (Right FAX) for After Final communications and 703-872-9310 (Right FAX) for customer service.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

Nitin Parekh  
05-10-03

*Aster Loke*